

IN THE SPECIFICATION

Please replace paragraph [0022] with the following:

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[0022] FIG. 2 is a diagram illustrating a preferred configuration of a memory section 22 of a DRAM integrated circuit. An example of a DRAM integrated circuit is a sixty-four Megabit ("Mb") DRAM array, where one Megabit is 2^{20} bits or 1,048,576 bits. FIG. 2 illustrates a 4 Mb memory section 22 of the DRAM array, sixteen of which comprise the 64 Mb DRAM integrated circuit. The memory section 22 may have a left neighboring section (not shown) and a right neighboring section (not shown). Sections 22 at the edge of the die of the DRAM integrated circuit ordinarily lack a left or right neighboring section. It should be understood that the DRAM array of the present invention is not restricted to the configuration of memory cells 10 in the DRAM array 20 as depicted in FIG. 2 and that other configurations of the DRAM array are possible. For example, each crossing of a bitline 16 and a wordline 18 may be connected to a memory cell 10.

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